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USING ELECTROMAGNETIC-BASED DESIGN SOFTWARE TO CHOOSE AND PLACE DECOUPLING CAPACITORS CAN MINIMIZE SWITCHING NOISE ON POWER AND GROUND PLANES.

Power-integrity and ground-bounce simulation of high-speed pc boards

As signal edge rates get faster, designers of today's high-speed digital pc boards encounter problems that were unimaginable a few years ago. At less than 1-nsec edge rates, the potential on the power/ground structure of a pc board can vary nonuniformly across the plane, corrupting the power supplied to ICs and resulting in logic errors. To ensure the proper operation of high-speed components, you need to eliminate variations in potential and maintain proper low-impedance power-delivery paths.

To achieve this goal, you need to position decoupling capacitors to minimize the amount of noise that high-speed signals produce on power and ground planes. Therefore, you need to know how many capacitors to use, what value each capacitor should have, and where to place each capacitor. Because you will likely need a large number of capacitors and board real estate is valuable, these details can make or break a design.

Trial and error are time-consuming and expensive, often resulting in overconstrained designs that unnecessarily increase manufacturing costs. Using software tools to analyze and optimize board design and board-real-estate usage provides a more practical means to test a greater variety of potential board configurations. This article illustrates this process for an xDSM (dense-subcarrier-multiplexing) board used in a fiber-optic/broadband-wireless network using Ansoft's SIwave, a full-wave, finite-element-based tool that imports board designs from layout tools such as Cadence Allegro, Mentor Graphics Board Station, Synopsys Encore, and Zuken CR-5000 Board Designer. **Figure 1** shows the layout of the board in SIwave. Because a pc-board structure is planar, SIwave can efficiently perform a thorough analysis. Outputs include board resonances, impedances, S-parameters on selected nets, and Spice decks.

The overall dimensions of the xDSM board, and therefore the power and ground planes, are 11×7.2 in. (28×18.3 cm). Both power and ground planes are 1.4-mil-thick copper separated by a 23.98-mil-thick substrate.

To understand the design of this board, first consider the behavior of a bare (unpopulated) xDSM board. Because of the expected rise times of the signals on this board, you need to understand its behavior in the frequency domain up to about 2 GHz. **Figure 2** shows the voltage distribution when a sinusoidal source excites the plane at 0.54 GHz. The board will also resonate at 0.81 and 0.97 GHz, as well as at higher frequencies. For better understanding, you can examine the voltage-distribution plots between the planes for each of the modes corresponding to these frequencies.

Figure 2 shows that the center of the board has a zero-voltage difference between the power and the ground plane for the mode at 0.54 GHz. The same situation is true for some additional higher order modes that the **figure** does not show, but it is not always true. On this board, a signal can excite high-

Figure 1

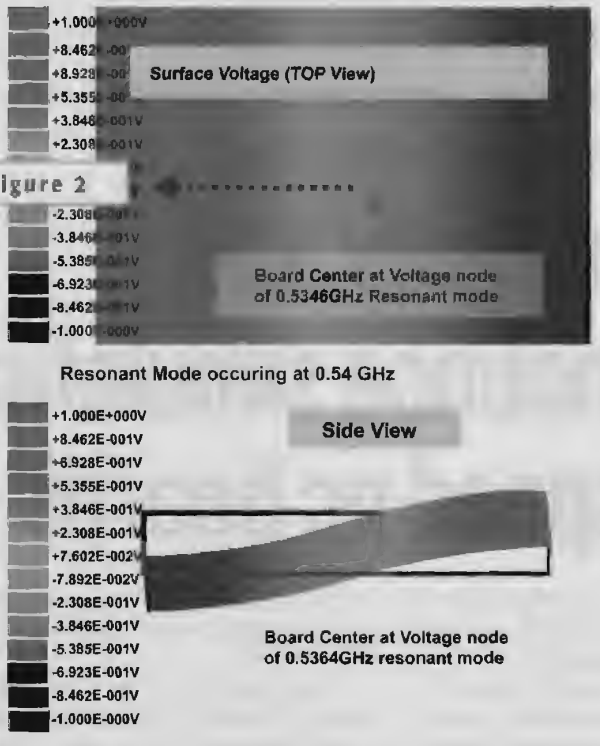
The xDSM board in SIwave contains two high-speed buses on the left side of the board and three Xilinx FPGA packages on the right side.

er order modes that are nonzero in the center of the board at 1.07, 1.64, and 1.96 GHz.

Understanding the location of the nulls is valuable for locating components that require large amounts of quickly changing current. For example, if you place a Xilinx FPGA IC that draws 2A in 0.2 nsec on a board, the large current and short rise time will create power-integrity problems if you allow them to excite modes that cause the voltage on the planes to be nonuniform. However, the fact that the center of the board is a null for these modes suggests that you can place the IC at the center of the board and not excite the lowest order mode. In this location, the IC cannot excite the lowest frequency mode because it is impossible to couple to this mode from the center of the board.

The purple line in **Figure 3** shows resonances when an IC draws current from the plane exactly in the center. Indeed, the first peaks are the higher order modes at 1.07, 1.64, and 1.96 GHz, as predicted—not at 0.54, 0.81, and 0.97 GHz.

Figure 2



This voltage distribution reveals the results when a sinusoidal source excites the plane at 0.54 GHz.

Although component location and placement can help reduce power-integrity problems, they are not panaceas. First, you cannot place all critical components at the center. Often, you have limited flexibility on component placement. Second, at any given location, some modes are excited, and others are not. For example, the green line in **Figure 3** shows what happens when you place this IC in a location off-center on one axis. For this placement, the lower frequency mode at 0.54 GHz also is excited. The key to successfully designing the PDS (power-delivery-system) is to add decoupling capacitors in the correct locations to achieve power integrity and low ground bounce over a sufficient frequency range.

DECOUPLING CAPACITORS

Given that the FPGA draws a current of 2A with a rise time of 0.2 nsec, the power voltage briefly drops (voltage droop), and the ground voltage briefly jumps (ground bounce). The magnitude of these effects depends on the impedance of the board and the capacity of the PDS to supply current at the location of the IC bias pin (**Figure 4a**).

Because the rapid current change is 2A, V=ZI provides the rapid voltage change, where Z is the impedance the chip "sees." Hence, to avoid an excessive spike in the voltage, the magnitude of Z must remain below a threshold for frequencies from dc to the bandwidth of the signal (**Figure 4b**).

In this example, the power-ground voltage difference must stay within 5% of the nominal value of 3.3V to maintain power integrity. Therefore, the noise cannot be more than 0.05×3.3V=165 mV. You find a conservative estimate of the maximum impedance of the PDS that the IC sees by applying Ohm's law. In this case, 165 mV/2A=82.5 mΩ—up to a frequency, f. The dotted lines in **Figure 4** indicate the target zone for the PDS impedance.

At the lowest frequencies—typically, 1 kHz or lower—the power supply satisfies the impedance requirement, and power and ground-plane structures typically do not degrade the impedance characteristics, because they have low resistance and inductance. At frequencies greater than 1 kHz, however, the inductance of the current path may be large enough to cause the voltage to exceed the limit, according to:

$$V = L\frac{di}{dt}.$$

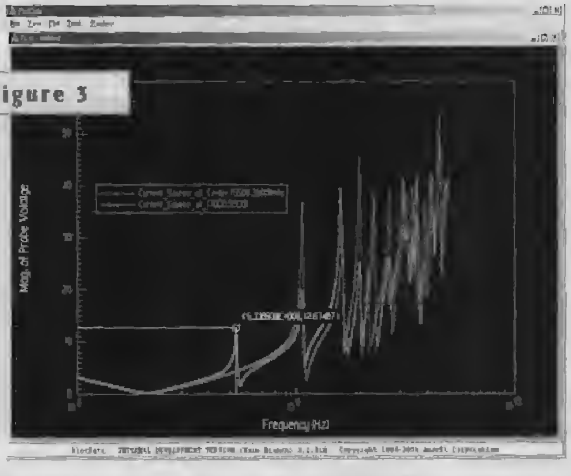
At higher frequencies, decoupling capacitors are necessary to provide a low-impedance connection between power and ground structures. The bandwidth, F, required for the PDS impedance is approximately:

$$F(GHz) = \frac{0.35}{T_{TRANSITION}(nSEC)},$$

or, in this case, 1.75 GHz.

Achieving such a broad bandwidth typically requires arrays of high-frequency ceramic capacitors for the megahertz region and electrolytic bulk capacitors for the kilohertz region. These capacitor arrays compete with other components for valuable board real es-

Figure 3



The purple trace shows the response of nearby voltage probes, as a function of frequency, when an IC at the center of the board draws a current; the green trace shows the response when you place the IC off-center.

tate. Virtual prototyping allows you to solve this problem without a physical prototype, which is necessary for a trial-and-error design methodology.

You can design a PDS for a pc board, such as the xDSM board in this example, using SIwave by placing a port at the IC and computing the input impedance of the board over the calculated bandwidth. The red line in **Figure 5** shows the impedance of the bare board without capacitors. Both the impedance scale and the frequency scale are logarithmic. This simulation shows the effect of the capacitance of the board itself and omits the low-inductance current return path through the power supply. Therefore, impedance increases as frequency decreases. However, because the path through the power supply has a low impedance, this relationship is not a concern.

The straight part of the red line indicates that the bare board has a capacitance of 74 nF, according to $Z=1/(j\cdot C)$. To bring the impedance below the limit of 82.5 mΩ at 1 MHz, the capacitance must be at least 2 µF—almost 30 times the capacitance of the bare board. The first attempt at achieving this goal results in the addition of an array of 22 0.1-µF capacitors. The dark blue line indicates the design's response. Over much of the frequency range, the design meets the impedance target. At the high end of the band, the ESL (equivalent series inductance), ESR (equivalent series resistance), and additional inductance representing the distance between capacitors cause the dark blue line to fail to meet the impedance requirement.

Because smaller capacitors have lower ESL and ESR values, adding bypassing can improve high-frequency performance. The light blue trace in **Figure 5** represents the addition of a second capacitor array having values of 10 nF each. The green trace represents a third array of 1-nF capacitors. Each array improves performance but still falls short of the requirement.

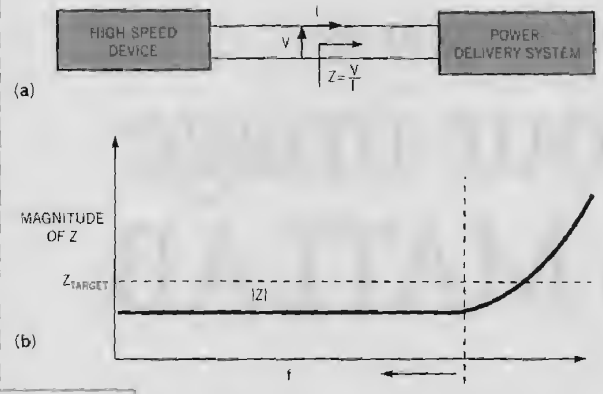


Figure 4 **The magnitude of effects depends on board impedance and capacity of the PDS the IC sees (a). To avoid an excessive spike in the voltage, the magnitude of Z must remain below a threshold for frequencies of dc to the bandwidth of the signal (b). Dotted lines indicate the target zone for PDS impedance.**

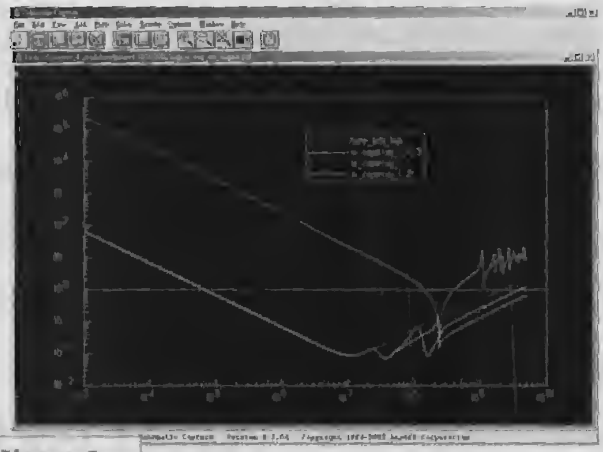


Figure 5 **The red trace shows the impedance of the bare board without capacitors. The dark blue line indicates the design's response, the light blue trace represents the addition of a second capacitor array having values of 10 nF each, and the green trace represents a third array of 1-nF capacitors.**

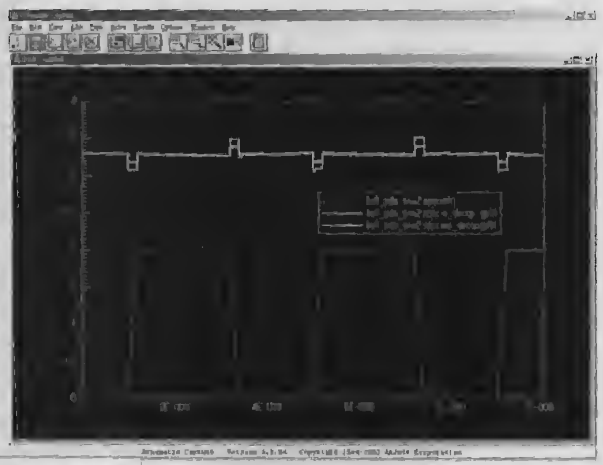


Figure 6 **In this depiction of power integrity before (blue) and after (green) the addition of the last series of capacitor arrays, the red line represents the current that the IC chip draws.**

At this stage of design, you can augment the electromagnetic simulator with a circuit simulator to complete the design. This approach allows you to more accurately model low-end impedance, including the loading effects of the power supply. It also allows you to simulate noise directly on the power pins, allowing you to verify the actual design goal (power-plane noise) and avoid over designing the device using conservative secondary design goals (power-plane impedance).

To begin, you add input and output ports in selected locations. A port is already on one of the ICs. You also add a port where a power source is connected and two ports in locations where other ICs are to be mounted. In SIwave, you perform a wideband frequency sweep and obtain the 4×4 scattering matrix of S-parameters over the entire range. Using Full-Wave Spice, you can then create a Spice-compatible circuit file and perform further analysis in the circuit-simulation environment.

In the completed circuit, the pc board is near the center of the circuit. The circuit also includes a model for the FPGA—a current source accompanied by a current probe and a differential voltage probe. Full-wave Spice creates a Spice circuit that includes the three capacitor arrays. Placing a fourth capacitor array at the IC further reduces the high-end impedance. The circuit also contains a dc power source with a small array of decoupling capacitors with values of 1 nF to 100 µF and additional models for two other ICs, as well as two small 100-nF capacitor arrays near these ICs.

Figure 6 shows the simulated noise on the supply voltage to the FPGA. The red line represents the rapidly changing supply current at the IC—a change of 2A in 0.2 nsec. The blue line represents the voltage at this IC before the addition of the last capacitor array. The deviation from 3.3V is small with this preliminary design, but it still exceeds the spec of 5%. The green line represents the voltage after the addition of the fourth array. The final design meets the specification with noise of less than 165 mV.

You can analyze other ICs on the board in a similar manner to ensure that they also do not suffer from the ill effects of power droop or ground bounce. In this example, the other ICs draw 100 and 50 mA, respectively, so their contribution to the noise is minimal.

Designing high-speed pc boards can be challenging. Proper board operation, for example, requires careful PDS design, which involves placing hundreds of decoupling capacitors and properly choosing their values and locations. Using a trial-and-error approach to optimize the power integrity of a pc board requires multiple design cycles and potentially higher cost compared with simulation of virtual prototypes.□

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